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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,933	04/30/2001	Bruce Leroy Beukema	ROC920010009US1	3353

26517 7590 09/24/2004

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EXAMINER	
SWEARINGEN, JEFFREY R	

ART UNIT	PAPER NUMBER
2143	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,933	BEUKEMA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. Swearingen	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6-8, 10, 15, 20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (U.S. Patent No. 4,918,686), hereafter referred to as Hayashi.

4. Pertaining to claim 1, Hayashi teaches communicating a port identifier [Figure 13 shows receiving information on a port with an id (e.g. item 162, input port IX) and comparing the port address (item 164)] from a first node to a second node coupled to the first node over a point-to-point network [Figure 6 shows a switch used in a data communications network that can be coupled to another switch], wherein the first node includes a plurality of network ports [Figure 6] and a plurality of communication registers [Figure 7A, Q1-Q4, queues are made up of registers], wherein each communication register is dedicated to an associated network port among the plurality of network ports and is configured to store data received over such associated network port [an output queue will receive and store data], and wherein the port identifier identifies a network port among the plurality of network ports to which the second node is coupled to the first node [Figure 13, item 162]; and
communicating data from the second node to the first node by initiating a write operation on the first node using the second node to store the data in the communication register associated with the network port identified by the port identifier [Figure 9A shows the "writing"

or transmitting of data from port S00' to port S35'. If two switches are connected to each other via their ports, then the output switch is the second node and the input switch is the first node.]

5. Pertaining to claim 6, Hayashi teaches communicating the data comprises sequentially storing a plurality of commands in the communication register associated with the network port identified by the port identifier, the method further comprising processing each of the plurality of commands in the first node [column 6, lines 40-42 and Figures 9A and 9B show the sequential transmission [storage] of data [commands]]

6. Pertaining to claim 7, Hayashi teaches initiating, with the second node, a read operation for a configuration register in the first node [column 7, line 34-65 disclose an Output Enable signal which enables the output of the queue [read operation], wherein communicating the node identifier is performed in response to the read operation [column 3, lines 60-63 disclose that each packet includes the target address [node identifier]]

7. Pertaining to claim 8, Hayashi teaches communicating the node identifier is in response to a read request sent over the point-to-point network by the second node [column 3, lines 60-63 disclose that each packet includes the target address [node identifier]. column 7, line 34-65 disclose an Output Enable signal which enables the output of the queue [read operation]. Since the Output Enable allows a packet to be transmitted with the node identifier or target address included, it is in response to a read request.]

8. Pertaining to claim 10, Hayashi teaches a plurality of network ports, each configured to couple a first node from a clustered computer system to another node in the clustered computer system over a point-to-point network [Figure 6];

9. a plurality of communication registers, each dedicated to an associated network port among the plurality of network ports and configured to store data received through such associated network port [Figure 7A]; and

10. a control circuit coupled to the plurality of communication registers and configured to automatically notify the first node in response to storage of data in any of the plurality of

communication registers [Figure 10, the PSTR1 and PSTR2 signals arrive when data arrives to be stored in an input queue T13 or T23, which are made up of registers]

11. Pertaining to claim 15, Hayashi teaches a control circuit that is configured to output a port identifier over a first network port among the plurality of network ports in response to a read request received over the first network port, the port identifier identifying the first network port as the network port from which the read request was received [Column 3, lines 60-63 disclose that each packet includes the target address [port identifier]. Column 7, line 34-65 disclose an Output Enable signal which enables the output of the queue [read operation]. Since the Output Enable allows a packet to be transmitted with the node identifier or target address included, it is in response to a read request.]

12. Pertaining to claim 20, Hayashi teaches a plurality of network ports, each configured to couple to another node in the clustered computer system over a point-to-point network [Figure 6];

a plurality of communication registers, each dedicated to an associated network port among the plurality of network ports and configured to store data received through such associated network port [Figure 7A]; and

a control circuit coupled to the plurality of communication registers and configured to automatically notify the node in response to storage of data in any of the plurality of communication registers [Figure 10, the PSTR1 and PSTR2 signals arrive when data arrives to be stored in an input queue T13 or T23, which are made up of registers]

13. Pertaining to claim 22, Hayashi teaches a plurality of nodes, each node including

a plurality of network ports [Figure 6]

a plurality of communication registers, each dedicated to an associated network port among the plurality of network ports and configured to store data received through such associated network port [Figure 7A]; and

a control circuit coupled to the plurality of communication registers and configured to automatically notify such node in response to storage of data in any of the plurality of

communication registers [Figure 10, the PSTR1 and PSTR2 signals arrive when data arrives to be stored in an input queue T13 or T23, which are made up of registers];

and

a plurality of point-to-point network interconnects, each coupled between a pair of nodes from the plurality of nodes through network ports on each of the pair of nodes [Figure 16A, EX designates a switch, or network node with network ports, and the arrows show the network interconnects.]

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2-5, 11-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, and further in view of Lyon (U.S. Patent No. 6,721,273).

16. Pertaining to claim 2, Hayashi teaches networking nodes together that have a plurality of ports and registers as applied to claim 1. Hayashi fails to disclose detecting storage of data in the communication register.

17. Lyon teaches detecting in the first node the storage of data in the communication register associated with the network port identified by the port identifier [Lyon shows a method of detecting a non-zero output of another logic device with a logical memory – a counter, in column 10, lines 17-19. A register is also a logic device with memory, and the method of detecting a non-zero output in the counter would work the same way on a register's output bits.]

18. Motivation exists to detect non-zero presence on a logic device with memory such as a register because data for a computing environment is typically not all zeroes. Data must contain information beyond just zeroes to include instructions and microprocessors are unable to execute instructions if they are not present in the data. The presence of all zeroes in the register would mean no data is present in the register to be transmitted, which means a non-zero presence would indicate the presence of data in the register. Therefore it would be obvious to someone of ordinary skill in the art to detect non-zero data on a register using the method of OR-ing the output bits of the logic device together as shown by Lyon.

19. Pertaining to claim 3, Hayashi and Lyon are applied as to claim 2. Hayashi fails to disclose generating an interrupt upon detecting storage of data in the communication register.

20. Lyon teaches generating an interrupt on the first node in response to detecting the storage of data in the communication register associated with the network port identified by the port identifier. Lyon shows a method of detecting a non-zero output of another logic device with a logical memory – a counter, column 10, lines 17-19. That method is combining the output bits of the logic device and OR-ing them together to get a single output [interrupt] that shows if there are non-zero states present in the memory device. A register is also a logic device with memory, and the method of detecting a non-zero output in the counter would work the same way on a register's output bits.

21. Motivation exists to detect non-zero presence on a logic device with memory such as a register because data for a computing environment is typically not all zeroes since that would mean no data is being transmitted, which means a non-zero presence would indicate the presence of data in the register. Therefore it would be obvious to someone of ordinary skill in the art to detect non-zero data on a register.

22. Pertaining to claim 4, Hayashi and Lyon are applied as to claim 3. Hayashi fails to disclose processing the interrupt and clearing the interrupt.

23. Lyon discloses processing the interrupt by processing the data stored in the communication register associated with the network port identified by the port identifier [column 6, lines 42-

47, PSRT1 is applied to the switch controller...in parallel with transfer of the packet, whereupon the switch controller...starts its control operation], and clearing the interrupt [The interrupt is generated by OR-ing the output bits of the register together. The registers are part of a queue, and as such will be emptied as their data is serviced and leaves the queue [transmitted]. When all bits have returned to the non-zero state [all data has been transmitted that is present in the queue] the OR interrupt will go away.]

24. Motivation exists to process the interrupt so that when data is detected, it will be used and removed from the queue without sitting around dormant. Motivation exists to clear the interrupt so the system does not keep processing and sending data when there is none to process and send. It would be obvious to one of ordinary skill in the networking art at the time of the invention to process and clear the interrupts showing that data is present in the switch taught by Hayashi.

25. Pertaining to claim 5, Hayashi and Lyon teach a switch with a plurality of communication registers and a way to detect data stored in those communication registers as applied to claim 4. Hayashi fails to disclose that the detection is for a non-zero value stored in the plurality of communication registers and resetting the plurality of communication registers.

26. Lyon discloses detecting the storage of data comprises detecting a non-zero value stored in any of the plurality of communication registers. [Lyon shows a method of detecting a non-zero output of another logic device with a logical memory – a counter, column 10, lines 17-19]. A register is also a logic device with memory, and the method of detecting a non-zero output in the counter would work the same way on a register's output bits. Lyon further discloses clearing the interrupt comprises resetting the plurality of communication registers to zero values. The interrupt is generated by OR-ing the output bits of the register together. The registers are part of a queue, and as such will be emptied as their data is serviced and leaves the queue [transmitted]. When all bits have returned to the non-zero state [all data has been transmitted that is present in the queue] the OR interrupt will go away.

27. Motivation exists to detect non-zero presence on a logic device with memory such as a register because data for a computing environment is typically not all zeroes since that would mean no data is being transmitted, which means a non-zero presence would indicate the presence of data in the register. Motivation exists to reset the registers to zero values after processing so that old data is not transmitted any more by the system. Therefore it would be obvious to someone of ordinary skill in the art to detect non-zero data on a register.

28. Pertaining to claim 11, Hayashi teaches a switch with communication registers, a plurality of ports, and a control circuit as applied to claim 10. Hayashi fails to disclose that the control circuit can detect the storage of data in a communication register.

29. Lyon discloses that a control circuit can be configured to detect the storage of data in a communication register among the plurality of communication registers by detecting a non-zero value stored in such communication register. Lyon teaches that the output bits of a counter, which is a logic device with a memory, can be logically OR-ed together to detect a non-zero presence, in column 10, lines 17-19.

30. Motivation exists to detect non-zero presence on a logic device with memory such as a register because data for a computing environment is typically not all zeroes since that would mean no data is being transmitted, which means a non-zero presence would indicate the presence of data in the register. Therefore it would be obvious to someone of ordinary skill in the art to detect non-zero data on a register.

31. Pertaining to claim 12, Hayashi and Lyon teach a switch with communication registers and a control circuit as applied to claim 11. Hayashi fails to disclose the first node will be automatically informed by generating an interrupt.

32. Lyon teaches the control circuit is configured to automatically notify the first node by generating an interrupt. Lyon detects a non-zero presence using an OR gate [column 10, lines 17-19]. The OR gate will give an output of "1" if anything non-zero is present. The output of "1" from the OR gate is considered an interrupt by the office.

33. Motivation exists to use the control circuit to notify the first node by generating an interrupt in order to have the node process any data present as quickly as possible to increase efficiency of the node and to cut down on network latency. It would be obvious to one of ordinary skill in the networking art at the time of the invention to send an interrupt to the first node upon detection of data in Hayashi's switch.

34. Pertaining to claim 13, Hayashi and Lyon are applied as to claim 12. Hayashi teaches a switch with a control circuit and communication registers. Hayashi fails to disclose the control circuit can generate a common interrupt for all registers.

35. Lyon discloses the control circuit is configured to generate a common interrupt for all of the plurality of communication registers. As previously applied, Lyon has taught that the output bits of a counter can be tied together with an OR gate to detect non-zero states [column 10, lines 17-19]. Examiner considers this generating an interrupt.

36. Motivation exists to apply an interrupt as taught in Lyon to a switch taught in Hayashi in order to have the node process any data present as quickly as possible to increase efficiency of the node and to cut down on network latency. Lyon teaches combining output bits of a digital device to check for a non-zero state. When combined with Hayashi, these output bits are output bits of a register, creating an interrupt output after OR-ing them together to show the presence of a non-zero state. Because of how digital logic works, it would be a simple technique from this point to tie the output bits of OR gates for each register together to allow for a common interrupt for all registers. It would be obvious to one of ordinary skill in the networking art at the time of the invention to extend the interrupt created by a register as previously applied to claim 12 to cover all registers by use of OR gates.

37. Pertaining to claim 14, Hayashi teaches a switch with a plurality of communication registers, a plurality of ports and a control circuit as taught in claim 10. Hayashi fails to disclose use of a logical-OR operation on all the binary outputs of the plurality of communication registers.

38. Lyon teaches that each communication register can include a plurality of binary outputs, and wherein the control circuit comprises at least one logic gate configured to generate an

interrupt signal by performing a logical-OR operation on all of the binary outputs of the plurality of communication registers as applied previously. When Lyon detects a non-zero presence using an OR gate, the OR gate will give an output of "1" if anything non-zero is present. The output of "1" from the OR gate is considered an interrupt by the office.

39. Motivation exists to generate an interrupt from the binary outputs of the communication registers in order to have the node process any data present as quickly as possible to increase efficiency of the node and to cut down on network latency. It would be obvious to one of ordinary skill in the networking art at the time of the invention to send an interrupt to the first node upon detection of data in Hayashi's switch.

40. Pertaining to claim 21, Hayashi teaches a switch with a plurality of ports, a plurality of communication registers and a control circuit. Hayashi fails to disclose the control circuit can generate an interrupt to notify a node of storage of data in the communication registers.

41. Lyon teaches the control circuit is configured to generate the notification by signaling an interrupt in response to any of the plurality of communication registers storing a non-zero value as applied previously. When Lyon detects a non-zero presence using an OR gate, the OR gate will give an output of "1" if anything non-zero is present. The output of "1" from the OR gate is considered an interrupt by the office.

42. Motivation exists to notify a node by generating an interrupt from the binary outputs of the communication registers in order to have the node process any data present as quickly as possible to increase efficiency of the node and to cut down on network latency. It would be obvious to one of ordinary skill in the networking art at the time of the invention to send an interrupt to the first node upon detection of data in Hayashi's switch.

43. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, and further in view of Murthy et al. (A 2Kx1K Space Switch ASIC for Use in Digital Exchanges, VLSI Design, 1994, Proceedings of the Seventh International Conference on, 5-8 Jan. 1994 Pages: 247 - 250).

44. Pertaining to claim 16, Hayashi teaches a switch with a control circuit and a plurality of registers as applied to claim 15. Hayashi fails to disclose a configuration register or that the control circuit can output data in the configuration register.

45. Murthy discloses a configuration register wherein the control circuit is configured to output data stored in the configuration register in response to the read request. Murthy has a Connection memory-CRAM which stores the switching information, Control Registers, and two RAM blocks for diagnostic purposes. This can be accessed through a microprocessor interface. [248].

46. Motivation exists to combine Murthy's configuration register with Hayashi's switch to aid in diagnosing errors [Murthy, 248] and tracking network intrusion [storing the switching information]. It would be obvious to one of ordinary skill in the networking art at the time of the invention to save the contents of a configuration register that was in use in a switch transmitting data over a network.

47. Pertaining to claim 18, Hayashi teaches a switch as applied to claim 10. Hayashi fails to disclose that the circuit can be made an integrated circuit device.

48. Murthy discloses that a switch can be made an integrated circuit device [Murthy teaches a switch implemented on an ASIC [page 247, column 1], which is a type of integrated circuit.]

49. Motivation would exist to implement Hayashi on an integrated circuit to save space in devices. Therefore it would be obvious to one of ordinary skill in the art to combine Hayashi and Murthy to implement a networking device as described by Hayashi on an integrated circuit.

50. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, and further in view of Peter Norton's Inside the PC (Eighth Edition, Indianapolis:Sams, 1999. 165.), hereafter referred to as Norton.

51. Pertaining to claim 9, Hayashi teaches a switch with a plurality of communication registers as applied to claim 1. Hayashi fails to disclose that the communication registers are allocated a range of register addresses and a write request may be sent to the register address.

52. Norton teaches the plurality of communication registers are allocated a range of register addresses in a register address space for the node, and sending a write request to the register address of the communication register associated with the network port identified by the port identifier. Norton shows a pointer register can refer to an address of a "region of memory" [communication register] that is used for a stack [queue].

53. Motivation exists to assign addresses to the communication registers in order for the stored data to be directly accessed. It is therefore obvious to one of ordinary skill in the networking art at the time of the invention to assign registers in Hayashi's switch to addresses as Norton teaches.

54. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi and Murthy, and further in view of Peter Norton's Inside the PC (Eighth Edition, Indianapolis:Sams, 1999. 165.), hereafter referred to as Norton.

55. Pertaining to claim 17, Hayashi and Murthy teach a switch with communication registers and a configuration register as applied to claim 16. Hayashi further discloses each communication register is configured to store data received over such associated network port [Figure 7A, Q1-Q4, queues are made up of registers and an output queue will receive and store data. Hayashi and Murthy fail to disclose allocating a range of register addresses to the plurality of communication registers.

56. Norton teaches the plurality of communication registers are allocated a range of register addresses in a register address space for the node, and sending a write request to the register address of the communication register associated with the network port identified by the port identifier. Norton shows a pointer register can refer to an address of a "region of memory" [communication register] that is used for a stack [queue].

57. Motivation exists to assign addresses to the communication registers in order for the stored data to be directly accessed. It is therefore obvious to one of ordinary skill in the networking art at the time of the invention to assign registers in Hayashi's switch to addresses as Norton teaches.

58. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi, and further in view of IEEE 100: The Authoritative Dictionary of IEEE Standard Terms (seventh edition, page 504), hereafter referred to as IEEE.

59. Pertaining to claim 19, Hayashi teaches a switching circuit as applied to claim 10. Hayashi fails to disclose that the switching circuit can be implemented in software describing the hardware.

60. IEEE teaches a program product comprising a hardware definition program that defines the circuit arrangement of claim 10. IEEE states that hardware description language is a general-purpose computer language designed to serve as an interface to the design, documentation, and validation of computer hardware. It would have been obvious and well known to one of ordinary skill in the networking art at the time of the invention to design a circuit using a hardware description language. It would have been obvious and well known to one of ordinary skill in the networking art to put a program on a signal bearing medium made up of a recordable medium such as a disk.

61. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. Swearingen whose telephone number is 571-272-3921 after 19 October 2004. The examiner can normally be reached on M-F 8:30-5:00

62. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 703-308-5221 (571-272-3923 after 28 October 2004). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

63. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to

the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey R. Swearingen
Examiner
Art Unit 2143

jrs

ZARNI MAUNG
PRIMARY EXAMINER